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1 IN THE SPECIFICATION

2 Please amend the specification as follows:

3 On page 6, replace the paragraph starting on line 16 with the following:

4 Referring now to Figure 2, in particular embodiments of the present invention, the network  
5 adapter 80 comprises a pluggable option card having a connector such as an edge connector for  
6 removable insertion into the bus architecture 70 of the host computer system 10. The option card  
7 carries an Application Specific Integrated Circuit (ASIC) or Integrated System on a Chip (ISOC)  
8 120 connectable to the bus architecture 70 via the connector 270 ~~170~~, one or more third level  
9 memory modules 250 connected to the ISOC 120, and an interposer 260 connected to the ISOC  
10 120 for communicating data between the media of the network architecture 30 and the ISOC 120.  
11 The interposer 260 provides a physical connection to the network 30. In some embodiments of  
12 the present invention, the interposer 260 may be implemented in a single ASIC. However, in  
13 other embodiments of the present invention, the interposer 260 may be implemented by multiple  
14 components. For example, if the network 30 comprises an optical network, the interposer 260  
15 may comprise a retimer driving a separate optical transceiver. The memory 250 may be  
16 implemented by SRAM, SDRAM, or a combination thereof. Other forms of memory may also be  
17 employed in the implementation of memory 250. The ISOC 120 includes a first and a second  
18 memory. The memory subsystem of the adapter 80 will be described shortly. As will become  
19 apparent from the following description, this arrangement provides: improved performance of  
20 distributed applications operating on the data processing network; improved system scalability;  
21 compatibility with a range of communication protocols; and reduced processing requirements in  
22 the host computer system. More specifically, this arrangement permits coexistence of  
23 heterogeneous communication protocols between the adapters 80 and the host systems 10. Such  
24 protocols can serve various applications, use the same adapter 80, and use a predefined set of  
25 data structures thereby enhancing data transfers between the host and the adapter 80. The number  
26 of application channels that can be opened in parallel is determined by the amount of memory

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1 resources allocated to the adapter 80 and is independent of processing power embedded in the  
2 adapter. It will be appreciated from the following that the ISOC 120 concept of integrating  
3 multiple components into a single integrated circuit chip component advantageously minimizes  
4 manufacturing costs and in provides reusable system building blocks. However, it will also be  
5 appreciated that in other embodiments of the present invention, the elements of the ISOC 120  
6 may be implemented by discrete components.

7 On page 14, replace the paragraph starting on line 14 with the following:

8 As indicated earlier, the transmission path logic 280 is responsible for processing transmission or  
9 outgoing frames. Frame transmission is initiated via the bus architecture 70 by a CPU such as  
10 CPU 50 of the host computer system 10. The ISOC 120 comprises bus interface logic 370 for  
11 communicating with the bus architecture 70. The ISOC 120 also comprises bus bridging logic  
12 ~~380~~ 390 connecting the bus interface logic 370 to a processor local bus (PLB) 390 of the ISOC  
13 120. The TX LCP engine 310 fetches commands and frames from the host memory 60. The TX  
14 processor 150 processes the header of each frame into a format suitable for transmission as  
15 packets on the network architecture 30. The TX logic 320 transfer the frame data without  
16 modification. The link logic 330 processes each packet to be transmitted into a final form for  
17 transmission on the network architecture 30. The link logic 330 may comprises one or more ports  
18 each connectable to the network architecture 30.

19 Replace the abstract on page 44 with the following:

20 Methods, apparatus and systems are provided for controlling flow of data between a memory of a  
21 host computer system and a data communications interface for communicating data between the  
22 host computer system and a data communications network. In an example embodiment, an  
23 ~~apparatus comprises~~ includes a descriptor table for storing a plurality of descriptors for access by  
24 the host computer system and data communications interface. Descriptor logic generates the

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- 1 descriptors for storage in the descriptor table. The descriptors include a branch descriptor
- 2 comprising a link to another descriptor in the table.

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